Claims

1. Method for making a field effect transistor comprising a source (10) and a drain (11) connected by a channel (7) controlled by a gate electrode (5) separated from the channel (7) by a gate insulator (3), the channel (7) being formed by a diamond-like carbon layer (1), method characterized in that it successively comprises

- deposition of a diamond-like carbon layer (1) on a substrate (2),
- deposition of an insulating gate layer (3) on the diamond-like carbon layer (1),
- deposition, on the insulating gate layer (3), of at least one conducting layer (4) and etching of the latter so as to form the gate electrode (5),
- deposition of an insulating material on flanks of the gate electrode (5) to form a lateral insulator (6),
- etching of the gate insulating layer (3),
- etching of the diamond-like carbon layer (1) so as to delineate the channel (7),
- deposition, on each side of the channel (7), of a semi-conducting material (9a) designed to form the source (10) and of a semi-conducting material (9b) designed to form the drain (11).

2. Method according to claim 1, characterized in that etching of the diamond-like carbon layer (1) is isotropic so as to obtain a retraction of the diamond-like carbon layer (1) under the gate insulating layer (3).

3. Method according to claim 2, characterized in that it comprises anisotropic etching of the semi-conducting materials (9a, 9b) in the zones of the substrate (2) not covered by the gate electrode (5) and the lateral insulator (6).

4. Field effect transistor comprising a channel (7) formed by a diamond-like carbon layer (1), transistor characterized in that it is obtained by a method according to any one of the claims 1 to 3.

5. Transistor according to claim 4, characterized in that the channel (7) comprises N-type dopants so as to form a PMOS type transistor (13).

6. Transistor according to claim 4, characterized in that the channel (7) comprises P-type dopants so as to form a NMOS type transistor (14).

7. CMOS logic gate, characterized in that it comprises PMOS type transistors (13, 14) according to claim 5 and NMOS type transistors according to claim 6, the PMOS and NMOS transistors having substantially the same dimensions.